Abstract of the Disclosure

A programmable logic device ("PLD") is augmented with programmable clock data recover ("CDR") circuitry to allow the PLD to communicate via any of a large number of CDR signaling protocols. The CDR circuitry may be integrated with the PLD, or it may be wholly or partly on a separate integrated circuit. The circuitry may be capable of CDR input, CDR output, or both. The CDR capability may be provided in combination with other non-CDR signaling capability such as non-CDR low voltage differential signaling ("LVDS"). THE CDR circuitry is provided with a programmable serializer and/or deserializer that can support higher data clock rates than the highest clock rate associated with the reference clock signal or clock signal from a phase locked loop circuit.